SP5070

2.GHz Fixed Modulus Frequency Synthesiser

DS3966-2.2 May 996

The SP5070 is a single modulus frequency synthesiser for use in Satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only an external transistor is required for varicap line driving.

FEATURES

- Low Power Consumption (5V, 47mA typ.)
- Prescaler and Preamplifier Included
- Charge Pump Amplifier with Feedback Point
- Charge Pump Disable Facility
- Synthesises Frequencies up to 2.4GHz
- Pin and Function Compatible with SP5060 and SP5062
- Full ESD Protection*

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems
- C-Band with Frequency Doubling Mixer

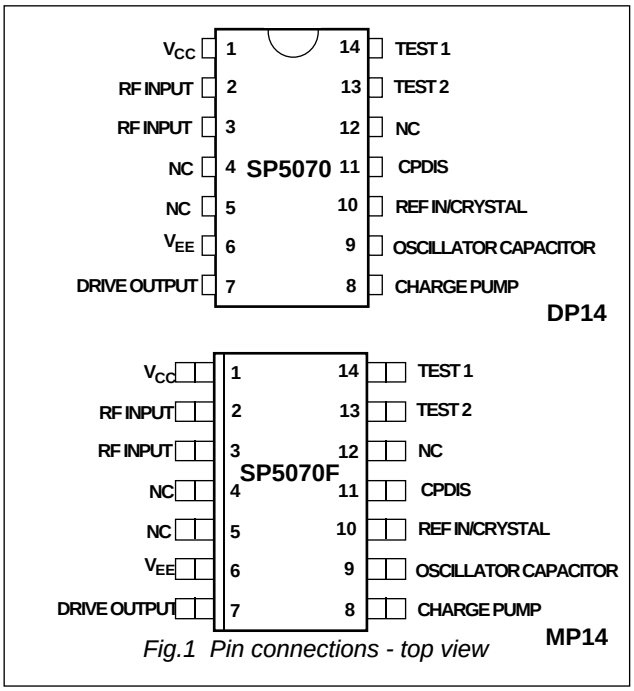

Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5070 DP - (14 Lead Plastic Package)
SP5070F MP - (14 Lead Miniature Plastic Package)

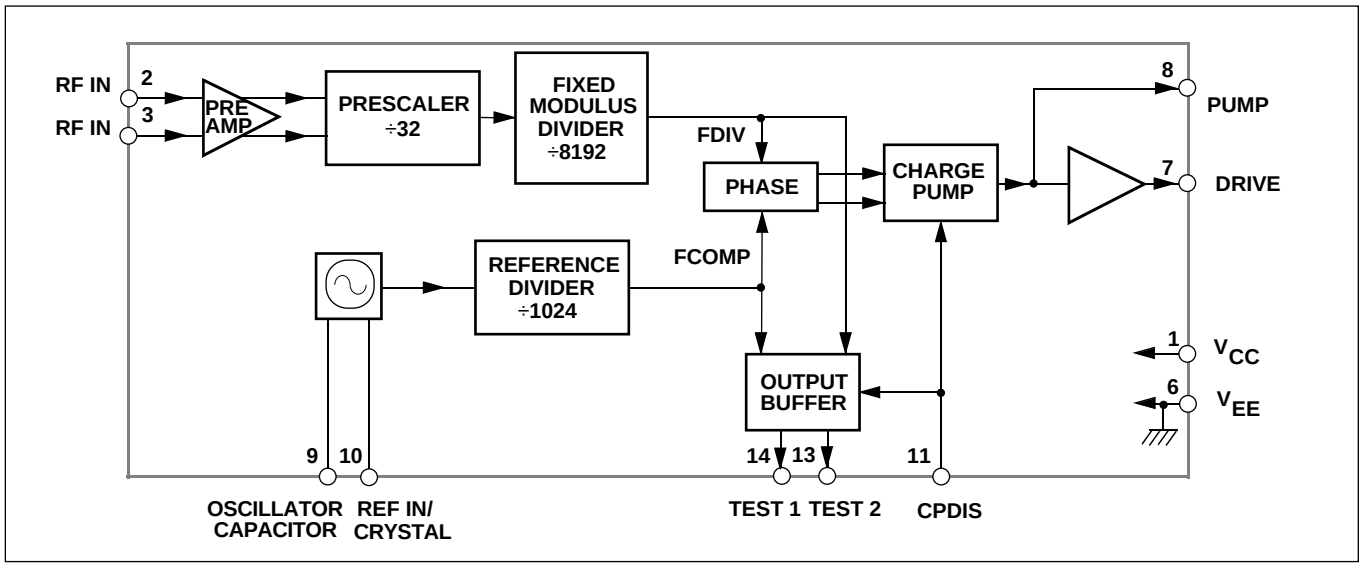

Fig.2 Block diagram of SP5070

ELECTRICAL CHARACTERISTICS

Tamb = -40°C to +85°C,VCC = +4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	1	-	47	55	mA	V_{CC} = 5V
Prescaler input voltage Prescaler input voltage		2,3 2,3	50 100	- -	300 300	mV_{RMS} mV_{RMS}	300MHz to 1.8GHz sinewave 2.4GHz, see Fig.5
Prescaler input impedance Input capacitance		2,3 2,3	- -	50 2	- -	Ω pF	
Charge pump output current Charge pump output leakage Drift due to leakage Charge pump drive output current Charge pump amplifier gain		8 8 - 7 -	- - - 1 -	±100 - - - 6400	- ±5 5 - -	µA nA mV/s mA -	V pin 8 = 2.0V V pin 8 = 2.0V At collector of External Varicap Drive transistor V pin 7 = 0.7V pin 7 current 100µa
Oscillator temperature stability Oscillator stability with supply voltage		9,10 9,10	- -	- -	2 2	ppm/°C ppm/V	
Reference clock frequency External reference amplitude		10 10	2 150	- -	10 500	MHz mV_{RMS}	
Charge pump disable/TEST 1 and TEST 2/enable Charge pump disable leakage		11 11	-250 -	- -	-500 10	µA µA	V_{IN}<0V V pin 11= V_{CC}
TEST 1/TEST 2 sink current		13,14	1	-	-	mA	VOUT = 0.7V
TEST 1/TEST 2 leakage current		13,14	-	-	10	µA	VOUT = V_{CC}+0.3V
TEST 1/TEST 2 voltage		13,14	-	-	V_{CC}+0.3	V	

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Characteristics	Pin	Value		Units
		Min	Max	
Supply voltage	1	-0.3	7	V
RF input voltage	2,3	-	2.5	Vp-p
RF input DC offset	2,3	-0.3	V_{CC}+0.3	V
Charge pump DC offset	8	-0.3	V_{CC}+0.3	V
Charge pump disable	11	-0.7	V_{CC}+0.3	V
Drive DC offset	7	-0.3	V_{CC}+0.3	V
Crystal oscillator DC offset	9,10	-0.3	V_{CC}+0.3	V
TEST outputs	13,14	-0.3	V_{CC}+0.3	V
Storage temperature	-	-55	150	°C
Junction temperature	-	-	+150	°C
DP14 thermal resistance, chip-to-ambient	-	-	78	°C/W
DP14 thermal resistance, chip-to-case	-	-	30	°C/W
MP14 thermal resistance, chip-to-ambient	-	-	123	°C/W
MP14 thermal resistance, chip-to-case	-	-	45	°C/W
Power consumption at 5.5V	-	-	275	mW

FUNCTIONAL DESCRIPTION

The SP5070, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator comparison frequency is obtained by dividing the reference frequency. This may be generated on-chip by means of an external crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phased locked to the comparison frequency.

The divider stages are arranged to give a fixed ratio between the synthesised frequency and the reference of 256:1. Any frequency within the range of 300MHz to 2.4GHz may be achieved by using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output drive necessary for the oscillator varicap line.

A test facility which disables the charge pump is also provided. This is activated when a negative voltage is applied to pin 11, see electrical characteristics above. When the device is in this mode, F_{COMP} and F_{DIV} are also available at outputs TEST1 and TEST2 respectively. These are open collector outputs and are each capable of sinking a minimum of 1mA. In normal mode of operation these outputs are high impedance.

For compatibility with SP5060/SP5062, pin 11 may be connected toV_{CC}

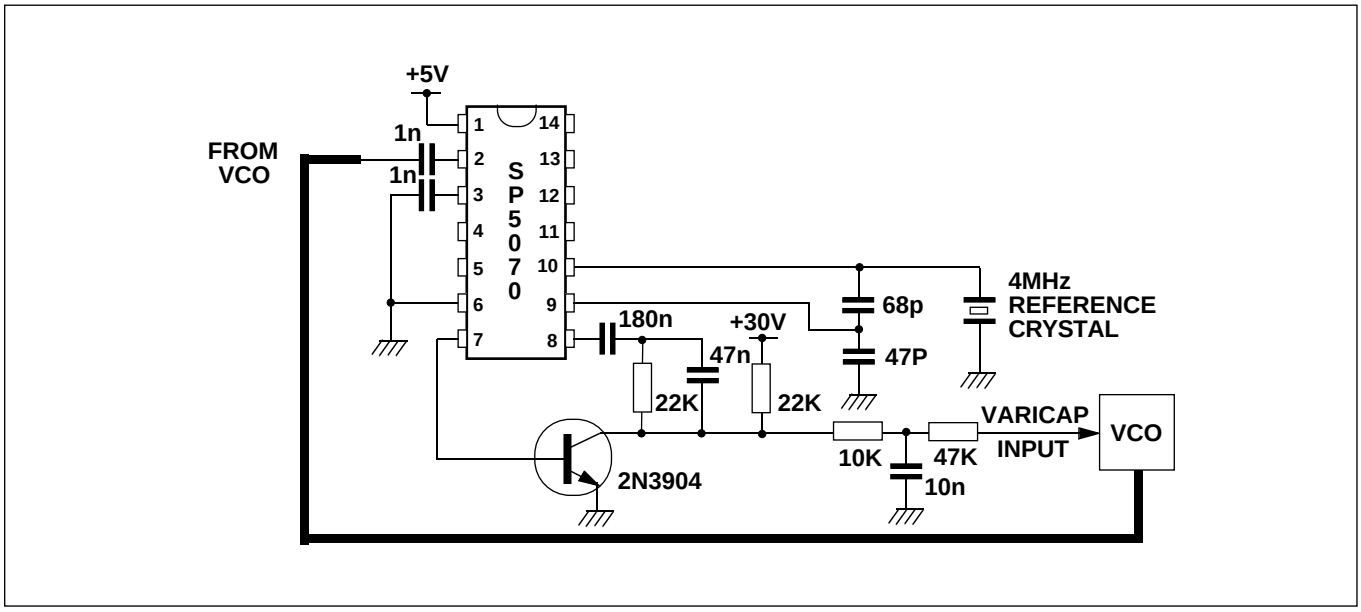

Fig.3 Typical application and test circuit (1024MHz with 4MHz reference crystal)

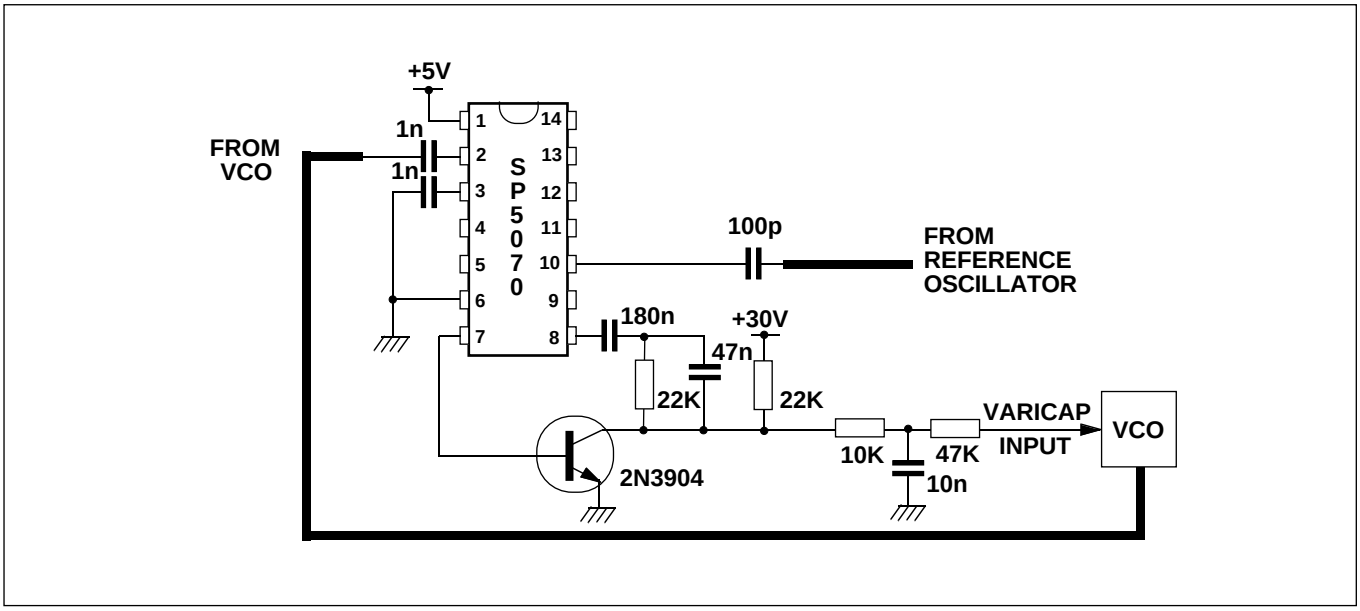

Fig.4 Application using external reference oscillator

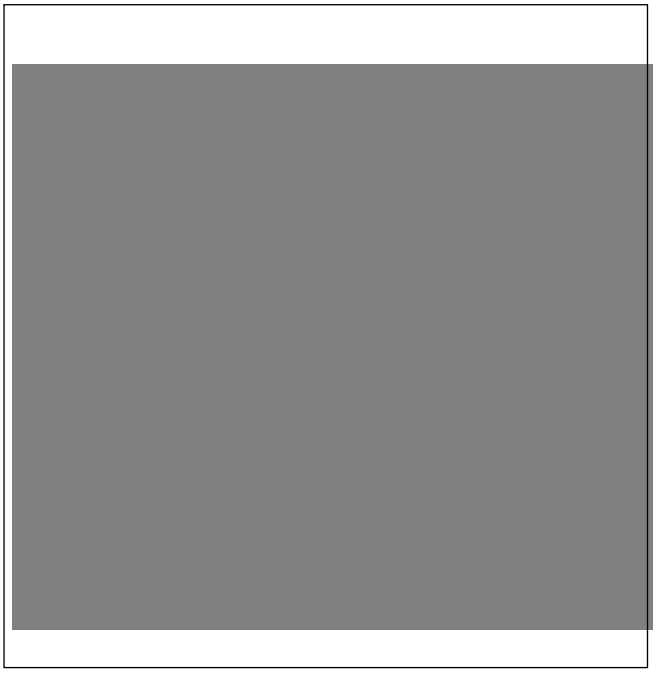

Fig.5 Typical input sensitivity

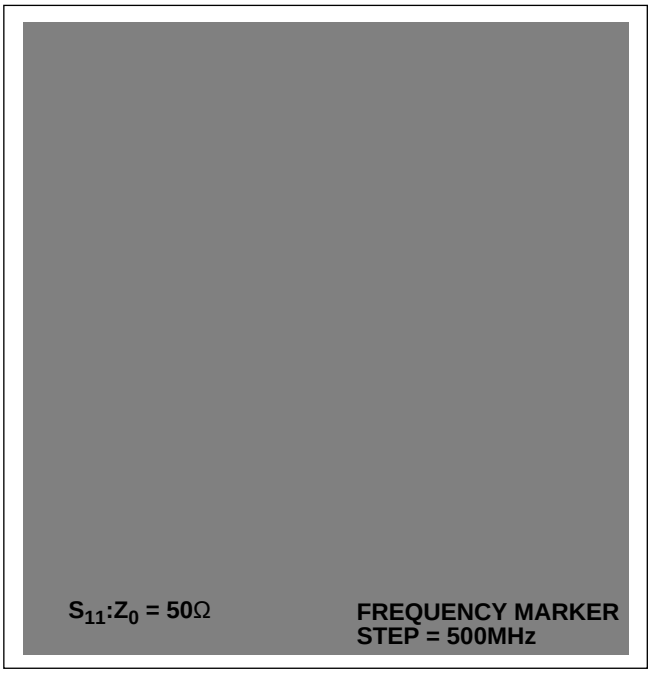

Fig.6 Typical input impedance

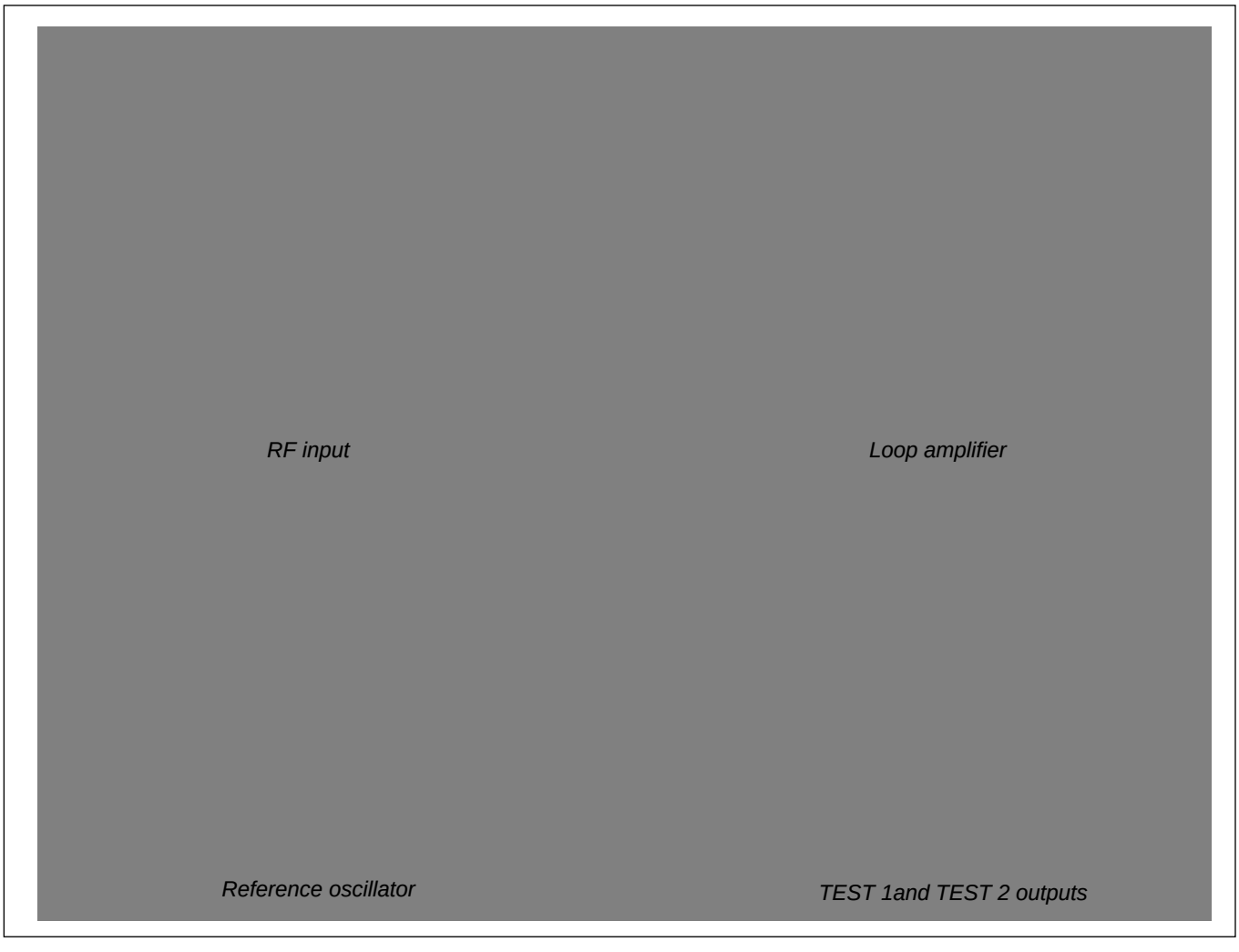

Fig.7 SP5070 input/output interface circuits

SP5070

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